OLLSCOIL NÁISIÚNTA NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SAMPLE Examinations 2014

CS4403 Introduction to Embedded Systems

An Scrúdaitheoir Eachtrannach
An Ceann Roinne
An Scrúdaitheoir Inmheánach

Answer QUESTION 1 and ONE other QUESTION

Total Marks: 80

1.5 Hours

The use of electronic calculators is permitted

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ENSURE THAT YOU HAVE THE CORRECT EXAM PAPER

QUESTION 1 (48 Marks)

(a) SP is a register that can be used as a pointer to a stack in memory. Rj is any register in a processor's register file. Load, Add, Subtract and Store are ISA commands in a RISC architecture. Write down the instruction sequences that implement the pseudocode (i) PUSH Rj and (ii) POP Rj

4 Marks

(b) Describe briefly how a memory operand can be addressed in a generic RISC computer Load instruction. Give one example. **4 Marks**

(c) Describe briefly what is being done by the following RISC code sequence

```
Move        R2, #LOC
LoadByte    R3,(R2)
LShiftL     R3,R3,#4
Add         R2,R2,#1
LoadByte    R4,(R2)
And         R4,R4,#0xF
Or          R3,R3,R4
StoreByte   R3,PACKED
```

4 Marks

(d) Write down the sequence of instructions that will put the 32-bit value 0x20004FF0 in register R2. Why is more than one instruction needed to do this? **4 Marks**

(e) An output display interface has a status register DISP_STATUS in which bit 2 is set when the output buffer is empty following transmission of a character to the display and cleared when DISP_STATUS is read by a program. Write an instruction loop, WRITEWAIT, to wait for an appropriate display status before writing a character to DISP_DATA. **4 Marks**

(f) A display output routine, WRITECHAR, is executed when an interrupt is received from the keyboard. Briefly outline the structure of the routine and the difference between it and the approach in part (e) above. **4 Marks**

(g) An interrupt routine needs to use registers R2 and R5 to contain a buffer address PNTR and an 8-bit value INDATA respectively. Write the instruction sequence to save these registers on the stack, put the PNTR and INDATA values in the registers and save the 8-bit value in the buffer addressed by PNTR. You may assume that the stack pointer, SP, has already been initialised.

4 Marks

(h) Describe, in words, the four steps into which execution of the instruction

ADD R3,R4,R5

can be subdivided. Why might an additional step be required for some instructions?

4 Marks

(i) List the 5 actions into which execution of a general instruction can be divided. List the five corresponding hardware stages. **4 Marks**

(j) Show in one diagram a conceptual view of the ALU segment of a RISC data path. Include input registers, output registers and any necessary multiplexers. Briefly outline the component functions. **4 Marks**

(k) Write a short paragraph on oscilloscope probe compensation as practised in your laboratory sessions. Sketch overcompensated, undercompensated and correctly compensated waveforms. **4 Marks**

(l) List the actions necessary in order to start up and run an Arduino Due sketch.

4 Marks

QUESTION 2 (32 Marks)

Use the following code sequence in part (a) of this question:

```
1. const int buttonPin = 2;
2. const int ledPin =  13;
3.
4. int buttonState = 0;
5.
6. void setup() {
7.
8.  pinMode(ledPin, OUTPUT);
9.
10.   pinMode(buttonPin, INPUT);
11. }
12.
13. void loop(){
14.
15.   buttonState = digitalRead(buttonPin);
16.
17.
18.
19.   if (buttonState == HIGH) {
20.
21.    digitalWrite(ledPin, HIGH);
22.   }
23.   else {
24.
25.     digitalWrite(ledPin, LOW);
26.   }
27. }
```

(a) Explain what this program does when it is uploaded to an Arduino card. Explain the purposes of lines 6, 10 and 13. What external circuitry would you use in connection with this sketch and how would you connect it? **9 Marks**

(b) The Arduino Due is based on an Atmel AT-SAM3X8E processor which itself contains an ARM Cortex M3 core. What is the maximum clock rate of the SAM3X? Describe the physical memory available on the Arduino AT-SAM3X. Give a general account of the Cortex-M3 architecture. **9 Marks**

(c) Describe bit banding in the context of the ARM Cortex-M3 **7 Marks**

(d) Describe the ARM Cortex-M3 Memory Map **7 Marks**

QUESTION 3 (32 Marks)

(a) The Intel Galileo board is an Arduino-compatible system based on the Intel Quark SoC X1000 Core. Give an overview of the memory layout. Draw a block diagram of the address translation mechanism.

10 Marks

(b) Give an account of the operating modes of the Quark core. **10 Marks**

(c) Based on your experience and knowledge of RISC and CISC processor design, write a short technical essay comparing the Intel Quark with the ARM M3 from the point of view of suitability for use in embedded systems.

12 Marks